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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,942	05/10/2001	Kikuo Ono	HITA.0052	4051

7590

06/20/2003

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EXAMINER

DUONG, THOI V

ART UNIT

PAPER NUMBER

2871

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/851,942

Applicant(s)

ONO ET AL.

Examiner

Thoi V Duong

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 ~~is~~/are pending in the application.
- 4a) Of the above claim(s) 6-8 and 12-21 ~~is~~/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ ~~is~~/are allowed.
- 6) ☒ Claim(s) 1-5, 9-11 and 22 ~~is~~/are rejected.
- 7) ☐ Claim(s) _____ ~~is~~/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ ~~is~~/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Supplemental Amendment, Paper No. 7, filed May 29, 2003 in response to the phone interview on April 29, 2003.

Accordingly, claims 2-4 were amended and new claim 22 was added in species IA. Applicant's election with traverse of Species IA, claims 1-5, 9-11 and 22 is acknowledged, where claims 1 and 9-11 are generic.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2, 9-11 and 22 are rejected under 35 U.S.C. 102 (e) as being anticipated by Kim et al. (USPN 6,091,466).

Art Unit: 2871

With respect to claims 1 and 9-11, as shown in Figs. 1-3, Kim et al. discloses a liquid crystal display device comprising:

a first insulating substrate 1 and a second substrate (not shown) being disposed so that respective main surfaces thereof are opposite to one another (col. 1, lines 38-40);

a liquid crystal layer being interposed between the first and second insulating substrates;

gate wiring lines 13 being formed on the first insulating substrate and transmitting scanning signals;

a gate insulating film 17 being composed of the first insulating substrate and the gate wiring lines;

drain wiring lines 23 being composed of metal films formed on the gate insulating film and transmitting video signals;

semiconductor layers 33 being formed on the gate insulating film and at least under the drain wiring lines;

thin film transistor sections , each of which has a semiconductor channel layer composed of a part of the semiconductor layer located at least over a part of the gate wiring layer, a drain electrode 21 composed of a part of the drain wiring line located on the semiconductor channel layer and a semiconductor contacting layer 35 formed of a part of the semiconductor layer being contacted with the part of the drain wiring lines, a source electrode 31 composed of another metal film formed on the semiconductor channel layer to be spaced from and opposite to the drain electrode and another

Art Unit: 2871

semiconductor contacting layer formed of another part of the semiconductor layer being contacted with a lower surface of the another metal film, and a protective film 37 covering the drain wiring lines, the source electrode, and the drain electrode; and pixel electrode sections, each of which has a pixel electrode 41 being contacted with the source electrodes, wherein

a planar pattern of each of the semiconductor layers is broader than those of the metal layers of the drain wiring layer, the source electrodes, and the drain electrodes formed thereon (Figs. 2D-2F), and

a planar pattern of each of the semiconductor layers 33 other than the semiconductor contacting layers 35 formed therein is broader than those of the semiconductor contacting layers (Figs. 2D-2F),

wherein the semiconductor channel layer is formed of non-impurity doped amorphous silicon, and the semiconductor contacting layer is formed of amorphous silicon doped with phosphorous (col. 2, lines 25-34);

wherein the metal layers of the drain wiring line, the source electrode, and the drain electrode are formed of chromium (Cr) (col. 2, lines 35-39); and

wherein the pixel electrode is formed of ITO, a transparent conductive film (col. 2, lines 66-67).

With respect to claims 2 and 22, as shown in Figs. 4 and 5A-5F, Kim et al. discloses a liquid crystal display device comprising:

a first insulating substrate 101 and a second insulating substrate (not shown) disposed to be opposite to the first insulating substrate (col. 1, lines 37-39);

a liquid crystal layer (not shown) being interposed between the first insulating substrate and the second insulating substrate (col. 1, lines 58-61);

a plurality of gate wiring lines 113, each of which is formed on the first insulating substrate and transmits a scanning signal;

a gate insulating film 117 being formed on the first insulating substrate and the plurality of gate wiring lines;

a plurality of drain wiring lines 123, each of which is formed on the gate insulating film and transmits a video signal;

a plurality of semiconductor layers 133, 135 and 133a, 135a being formed on the gate insulating film and at least under one of the plurality of drain wiring lines;

thin film transistor sections provided for respective pixels, each of thin film transistor section has a semiconductor channel layer formed of a part of the one of the plurality of semiconductor layers extended at least over a part of one of the plurality of gate wiring lines, a drain electrode 121 formed of a part of the one of the plurality of drain wiring lines situated on the semiconductor channel layer, a source electrode 131 formed on the semiconductor channel layer at an opposite side of the part of the one of the plurality of gate wiring lines to the drain electrode to be spaced from the drain electrode; and

a protective 137 made of organic insulating material and covering the plurality of drain wiring lines, the source electrodes, and the drain electrodes (col. 6, lines 11-25), wherein

each of the respective pixels has a pixel electrode 141 formed on the protective film and contacted with the source electrode of one of the thin film transistor sections through a first contact hole 171 perforating the protective film and a charges-holding capacitance section having an upper electrode 151 connected to one of the pixel electrode through a second contact hole 181 perforating the protective film and a lower electrode formed of another of the gate wiring line 113 or a material thereof (col. 6, lines 3-10),

a dielectric film being interposed between the lower electrode and the upper electrode of the charges-holding capacitance section includes at least the gate insulating film 117 (col. 6, lines 3-10), and

the charges-holding capacitance section is provided with another of the plurality of semiconductor layers (133a, 135a) having a planar outline inside which the second contact hole is located and being contact with the pixel electrode,

wherein the dielectric film interpose between the lower electrode and the upper electrode at the charges-holding capacitance section also includes the another of the semiconductor layers (Fig. 5F).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USPN 6,091,466) in view of Rho et al. (USPN 6,243,146 B1).

Kim et al. discloses a LCD device that is basically the same as that recited in claims 3 and 4 except for the pixel electrode being contacted with the gate insulating film through the second contact hole which is provided by perforating the semiconductor layer at the charges-holding capacitance section. As shown in Figs. 2E and 2F, Kim et al. discloses a conventional LCD device wherein a pixel electrode 41 contacts with the a gate insulating film 17 through a second contact hole 81 which is provided by perforating a passivation film 37 and the storage capacitor electrode 51 at the charges-holding capacitance section. As known in the art, the storage capacitance will be increased since a dielectric film includes only the gate insulating film (see USPN 6,243,146 B1 of Rho et al., col. 2, lines 38-53 and Fig. 17B). Thus, it would have been obvious to form a pixel electrode to contact with the gate insulating film by perforating the semiconductive layer at the charges-holding capacitance section so as to increase the storage capacitance.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USPN 6,091,466) in view of Lyu et al. (USPN 6,001,539).

Kim et al. discloses a LCD device that is basically the same as that recited in claim 5 except for the protective film of the thin film transistor formed by stacking an inorganic material film and an organic material film. As shown in Fig. 2B, Lyu et al. discloses that a protective film of the conventional LCD has a layered structure having organic and inorganic films 10, 15. The inorganic insulating film is formed on the organic

Art Unit: 2871

film prior to forming pixel electrode 12 in order to improve adhesion between the pixel electrode and the organic film (col. 1, lines 55-67). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LCD device of Kim et al. with the teaching of Lyu et al. by forming a protective film of the thin film transistor consisting of an inorganic material film and an organic material film so as to obtain a good adhesion to the pixel electrode.

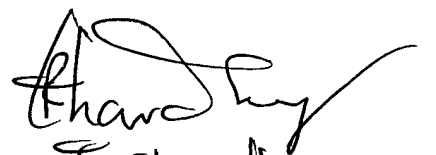
Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong

06/06/2003


Thoi Duong
Primary Examiner